REMARKS/ARGUMENTS

Reexamination of the captioned application is respectfully requested.

A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicants basically:

1. Editorially amend the specification.
2. Cancel original claims 1 – 14 without prejudice or disclaimer.
3. Add new claims 15 – 32.
4. Respectfully traverse all prior art rejections.

B. THE NEW CLAIMS

The new claims are entirely supported by the original disclosure including the original claims.

C. PATENTABILITY OF THE CLAIMS

Claims 1-13 stand rejected under 35 USC §103(a) as being unpatentable over Patil et al., "Efficient Run-Time Monitoring Using Shadow Processing" (see enumerated paragraph 8, page 3+ of the Office Action) in view of US Patent 4,530,051 to Johnson et al. All prior art rejections are respectfully traversed, particularly with reference to the new claims 15 – 32 which clarify distinctions including those noted below.

The primary applied reference (Patil) is directed to an entirely different situation than that claimed by Applicants. Patil relates to a performance monitoring system wherein a second "shadow" process (comprising all or part of a particular first actual process) is to run on a different processor more or less simultaneously or to some extent in parallel with the first process. Patil's arrangement allows separate monitoring of the first process (or part thereof) without intervening with the operation of the first actual process. Of course, by operating the second process as a "shadow" of the actual first

process on a different processor from which the first actual process operates on, the "main" processor on which the first actual process operates will be largely relieved of the burden of operating the second "shadow" process and of providing additional functionality that may be associated with the operation of the second "shadow" process.

In contrast to Patil, Applicants do not operate the same process, or part thereof, on different processors regardless of whether such processes, or any part thereof, are operated at the same time or in parallel, or not. The term "shadow" as used in Applicants' specification is more like a "silhouette" since it covers a situation wherein for a first actual process residing or operating on one processor (which first actual process requires interaction with a second actual process residing on a different processor) there is a co-located "shadow" process that merely is a representative of the second actual process. Applicants' "shadow" process is provided with an identity and an inter-process signal communication interface that is the same as that of the actual process that is represented by the "shadow".

Accordingly, to its local environment Applicants' "shadow" process appears to be the actual process. As such, the "shadow" will be the target of a signal from a co-located process in a case where the signal is intended for an actual process that is residing on the different processor. These particular properties of the interface of the "shadow", that are presented to other co-located processes, in conjunction with the task of the "shadow" of communicating the signal to a co-located actual process or to a "shadow" process on a different processor, generally constitutes a set of simple tasks of small volume with low resource demands compared to those of the actual process for which the "shadow" process is a representative.

Applicants' "shadow" of an actual process does itself not provide any of the substantive functionality that actually is provided by the corresponding actual process. Rather, the "shadow' provides an interface to any other process residing on the same

processor, that for process interaction is the same as the interface of the corresponding actual process (which, consequently, resides on a different processor).

Thus, Applicants achieve a distribution of constituent processes of a complex multi-process program over a plurality of interconnected processors, that each has its own operating system. Applicants do not require any extensive reconfiguration with regard to the multi-process architecture or the individual processes. Instead, the task performed by the "shadow" is merely to communicate a signal to or from a peer "shadow" residing on a different processor, or an actual process residing with the "shadow", which typically only takes a very small amount of processor resources compared to the resource usage of the corresponding actual process.

Applicants have reviewed the references cited by the Examiner and believe that none provide a basis for denying patentability of Applicants' pending claims. Please note that the pending claims are new claims which set forth more perhaps poignant features noted in the above discussion. In view of the foregoing explanation and new claim language, Applicants trust that it will be clear to the Examiner that neither Patil, US Patent 4,530,051 to Johnson, nor any alleged (improper) combination thereof teaches or suggest the claimed subject matter.

Applicants below address only some of the incorrect assertions of the Office Action levied with respect to some claims. Applicants reserve the right to address other assertions in the future should the need arise.

With reference to the original patent claim 1, the Examiner incorrectly observes that "one of ordinary skill in the art will be motivated [to modify the shadow process system of Patil such that the utilizes the arrangement for inter-processor or inter-computer process signal communication in a system comprising two or more CPUs or computers] because it simplifies the task of invoking or calling for execution of the

different procedures required to execute the process because the actual processes are statically associated with the home processor while the shadow process which are identical to that of the actual process will reside on a remote processor."

Applicants vigorously disagree. As explained above, the shadow process of the present invention is in no way identical to that of the actual process residing on a remote processor. Applicants represent a technical solution that is significantly different from the art taught by either Patil or Johnson.

Concerning original claim 9 the Examiner quotes from Patil (Fig. 1 and Fig. 4, page 1, paragraph 3): "a basic idea is to partition an executable program into two run-time processes as shown in figure 1. One is the main process, executing as usual. The other is a shadow process. The two processes may communicate and synchronize during execution".

Yet, this quote does not address the fact that Patil does not indicate or give any hint of an arrangement where two processors in a system for distributed data processing both are hosting respective shadow processes in the sense claimed by Applicants, and that the communication in fact takes place between the shadow processes, rather than between the actual process on one processor and a corresponding shadow process on a different processor as disclosed by Patil. This responsive consideration also applies to the alleged grounds presented for rejecting original patent claim 7. In the Office Action, the Examiner referenced Patil, Figure 2, page 3, section 2, quoting "Each pointer in the main process has a guard G_p in the shadow. The guard for a pointer stores spatial and temporal attributes for the pointer's referent".

With all due respect, Applicants submit that the Examiner's combination of Patil and US Patent 4,530,051 to Johnson and the further modifications required would only be possible using hindsight after reading Applicants' disclosure. One example telling

indication of hindsight appears in the last paragraph of the section of the Office Action which refers to original claim 13, which concludes: "One of ordinary skill in the art would be motivated to do so because it simplifies the task of invoking or calling for the execution of the different procedures required to execute a process because the actual processes are statically associated with the home processor while the shadow processes which are identical to that of the actual processes will reside on a remote processor. This improvement over the prior art would eliminate the need for intra process messages to be sent among different processors and allow the execution of a process by two or more processors without substantial increase in system overhead."

From the foregoing it also appears that the Examiner has not correctly understood the technical challenge and problem solved by Applicants nor the manner of doing so. Applicants in a simple way facilitate the distribution of individual processes that constitute a complex processing system over a number of interconnected processors or computers without having to rearrange the architecture of the complex program with respect to the identities of the various processes of the program, regardless of which processor is assigned to a particular process. Naturally, the overall effect of distributing the constituent processes of a multiprocess computer program over a plurality of processors typically is a reduced work load on each participating processor, although this is an advantageous effect which is common to most systems for distributed processing. In this regard does the present invention represent a further technology enhancement in the field of distributed processing.

Applicants respectfully submit that no reference of record provides a basis for denying the patentability of Applicants' claims. It is respectfully requested that all rejections be withdrawn and the application passed to issue.

D. MISCELLANEOUS

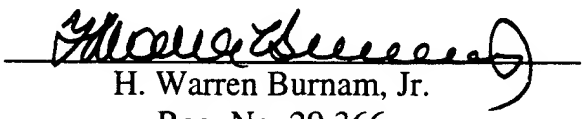
In view of the foregoing and other considerations, a formal indication of allowance is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
H. Warren Burnam, Jr.
Reg. No. 29,366

HWB:lsh
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100